A Novel Approach To Dual Damascene Patterning

Makarem Hussein, Sam Sivakumar, Ruth Brain, Bruce Beattie, Phi Nguyen, and Mark Fradkin

Portland Technology Development
Intel Corporation
Hillsboro, Oregon

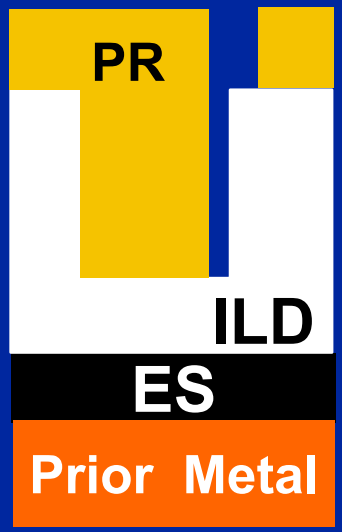
Outline

- Key patterning challenges
- BOARC-assisted patterning
- Innovative approach to patterning
- Conclusion

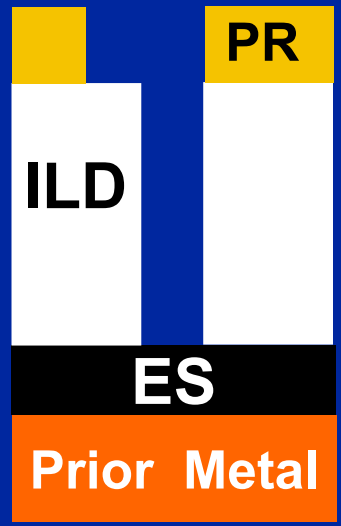
Outline

- **Key patterning challenges**
- BOARC-assisted patterning
- Innovative approach to patterning
- Conclusion

Patterning Approaches

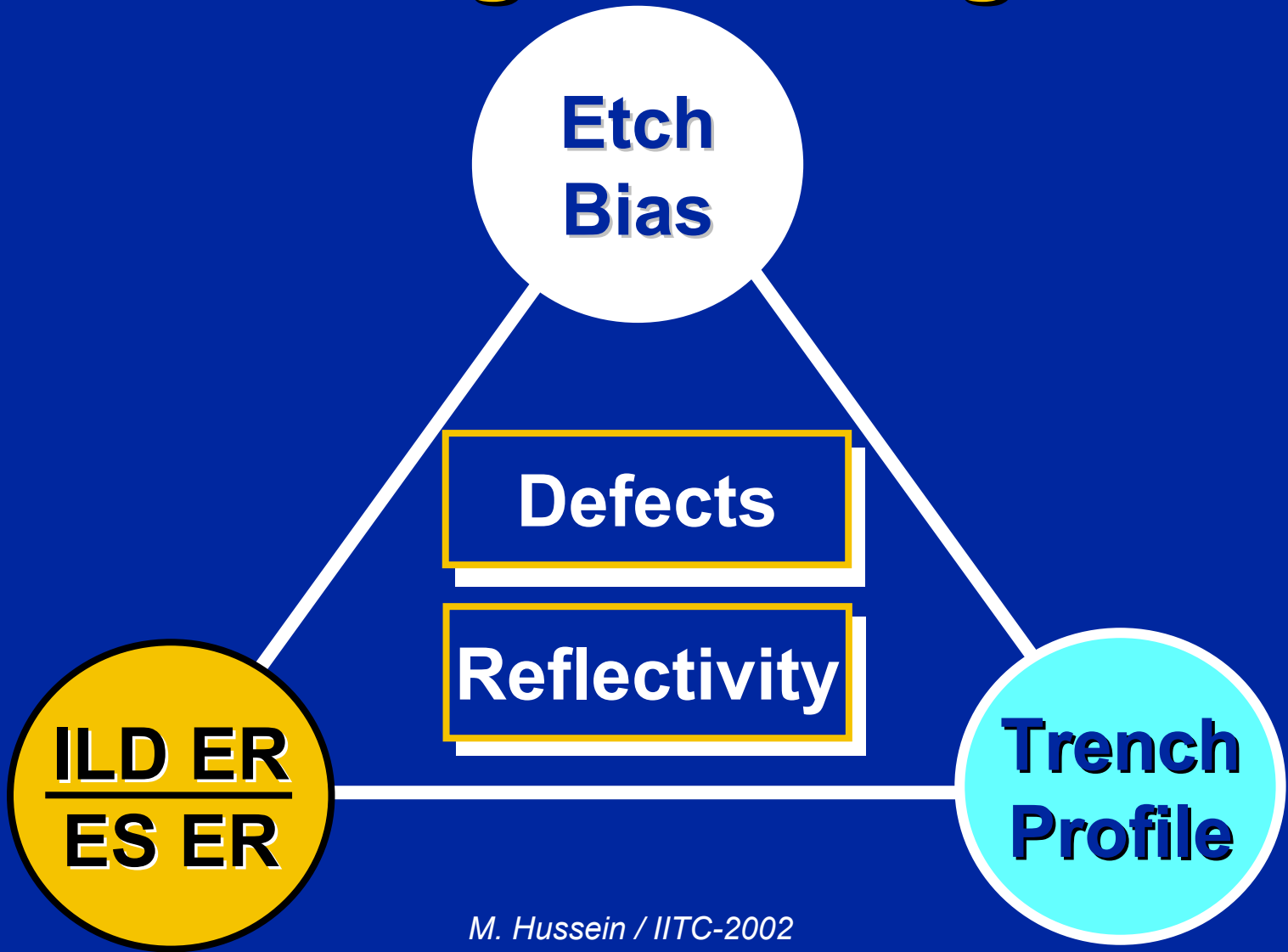


- Trench First
 - Un-landed via
 - Defects

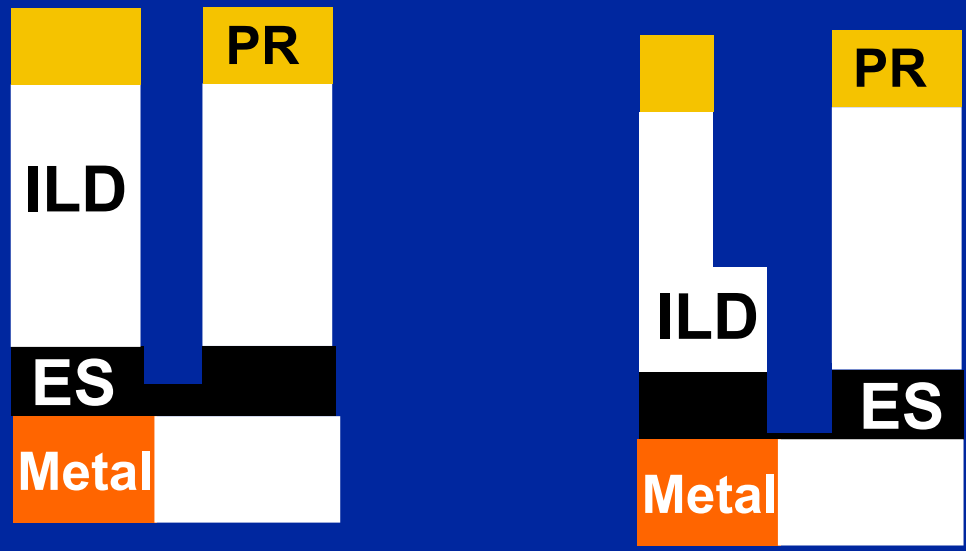


✓
- Via-First
 - Selectivity to ES
 - Defects

Patterning Challenges



Problem: Selectivity to ES

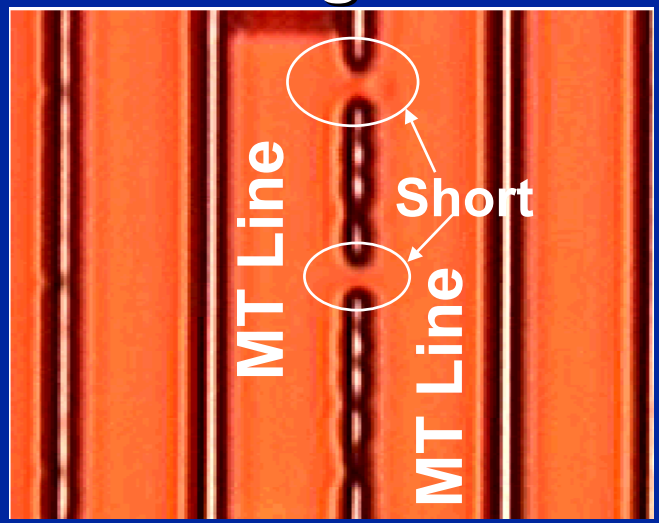


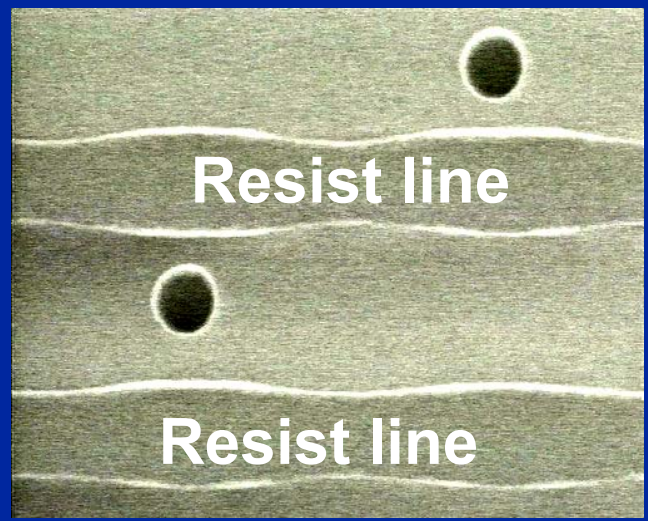
- ES layer must be thick enough to:
 - Protect Cu during via & trench etch and cleans
- ES layer must be thin enough to reduce impact on integrated dielectric constant

Impractical selectivity requirement!

Problem: Reflectivity

- Higher than 30% (1 σ) reflectivity variation seen on ILD substrate at litho
- WIW variations in substrate reflectivity causes significant local reflections



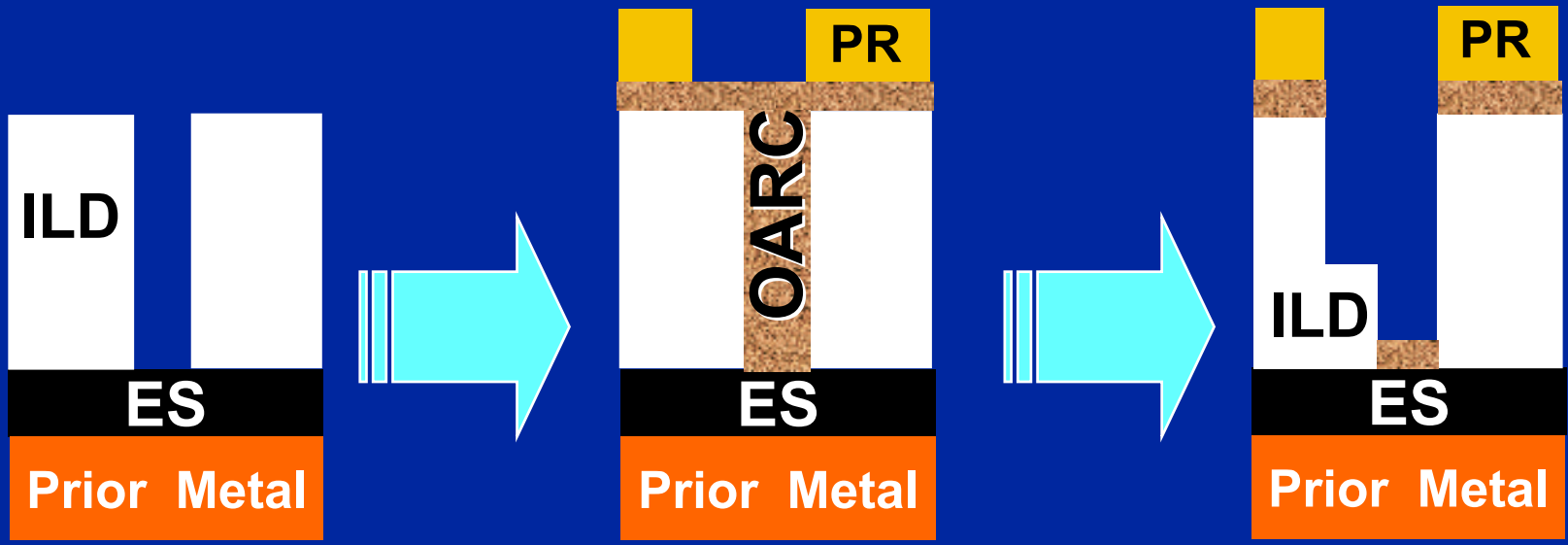


Reflectivity control is needed

Outline

- Key patterning challenges
- **BOARC-assisted patterning**
- Innovative approach to patterning
- Conclusion

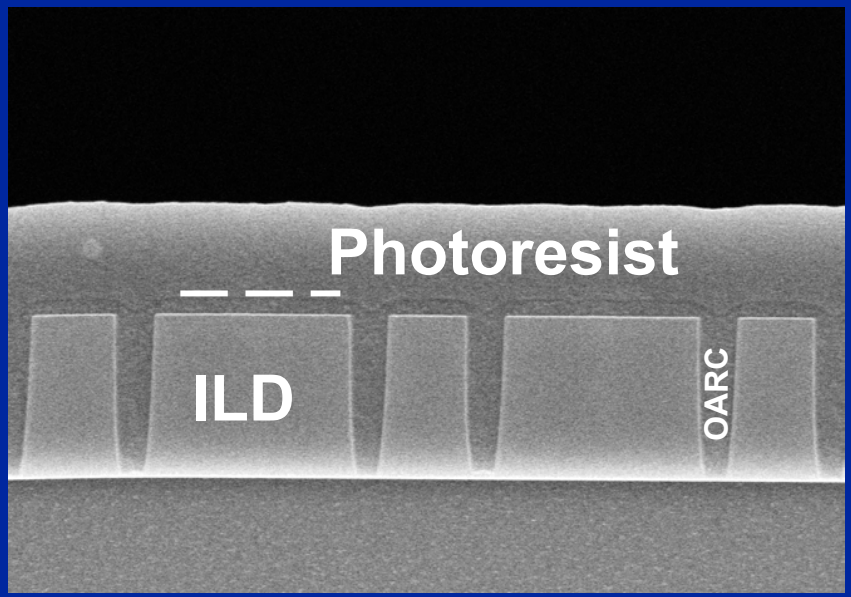
The BOARC Solution

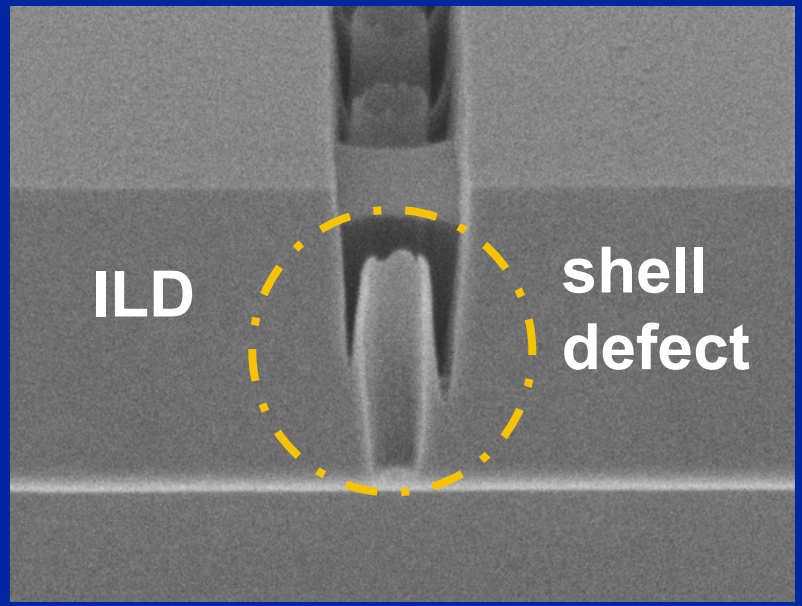


- BOARC solves the reflectivity problem and relaxes ES selectivity requirement

ALL AT THE EXPENSE OF DEFECTS

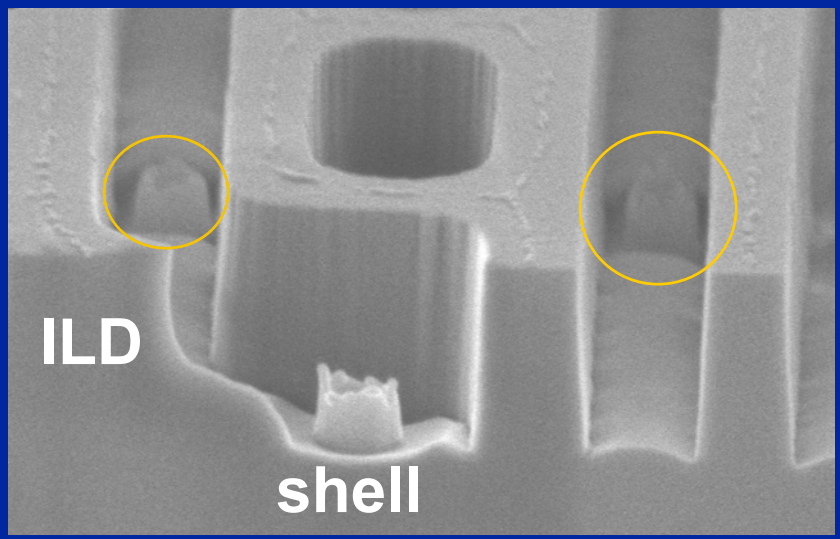
BOARC-Induced Defects

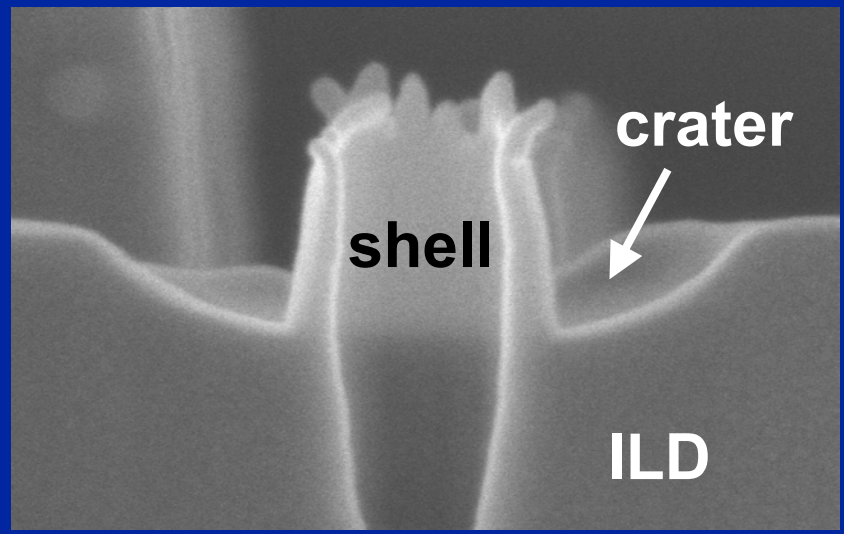




- ILD trench etch rate > BOARC etch rate
- Shell defect is formed

Defect Is Hard To Remove

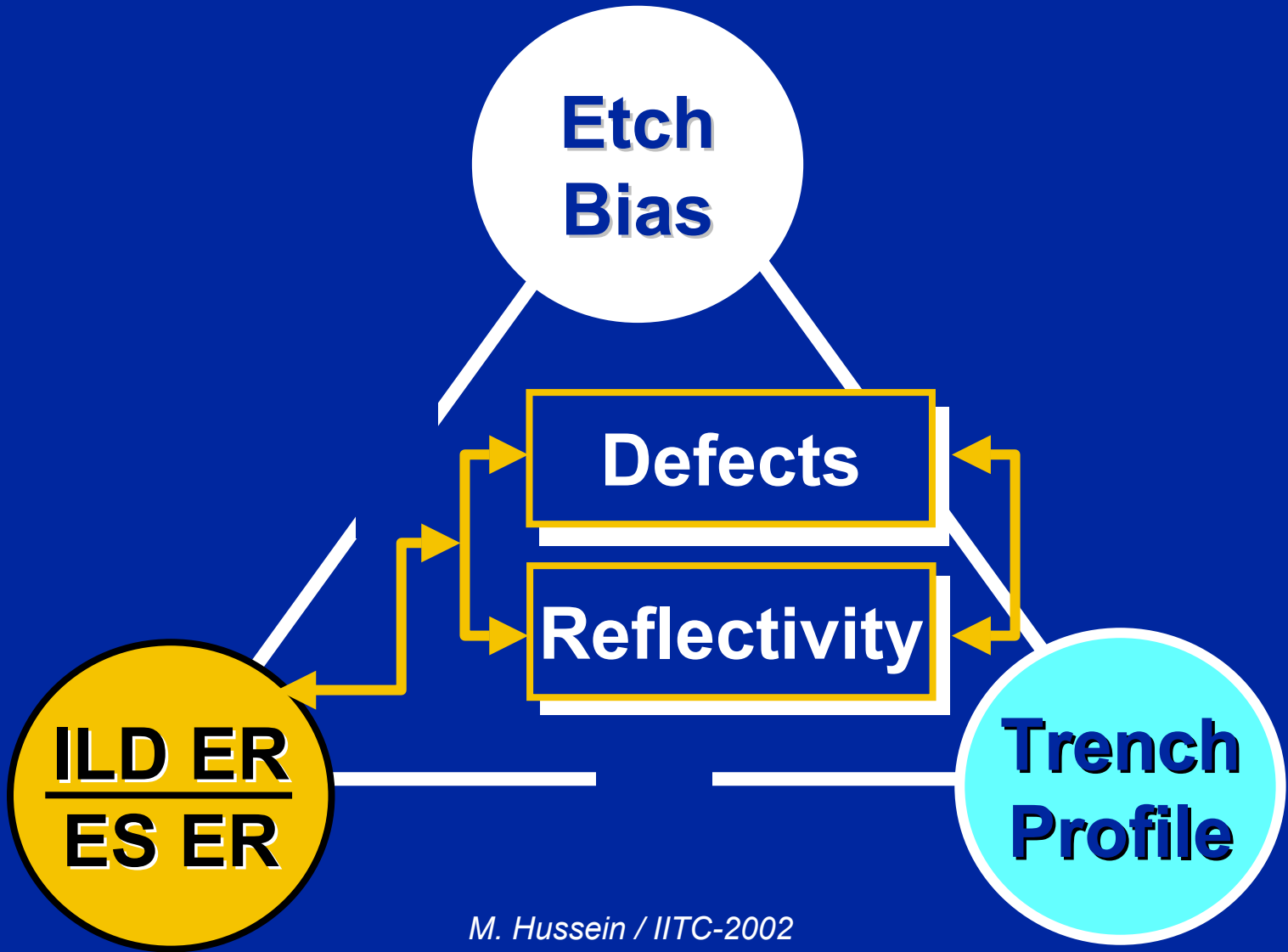




Unsuccessful attempts to remove shell defect:

- **Trench etch process modification**
- **Post trench etch cleans**

An Invention Is Needed!



Outline

- Key patterning challenges
- BOARC-assisted patterning
- **Innovative approach to patterning**
- Conclusion

The Ultimate Via Fill

- Vias should be filled with a material prior to trench litho:
 - Protects the ES layer during trench etch
 - Provides trench litho with a “hole-free” surface
- The via fill material should be highly absorbing to suppress substrate reflectivity
- The via fill material etch rate should be comparable to that of the ILD
 - Avoid formation of shell defect

The ultimate via fill material does NOT exist…

It has to be invented …

Introducing SLAM

- SLAM is Sacrificial Light Absorbing Material used as a via fill
- SLAM is synthesized by adding a light absorbing dye to a member of the siloxane family of spin-on-glass
- SLAM is applied by spin coating with standard bakes

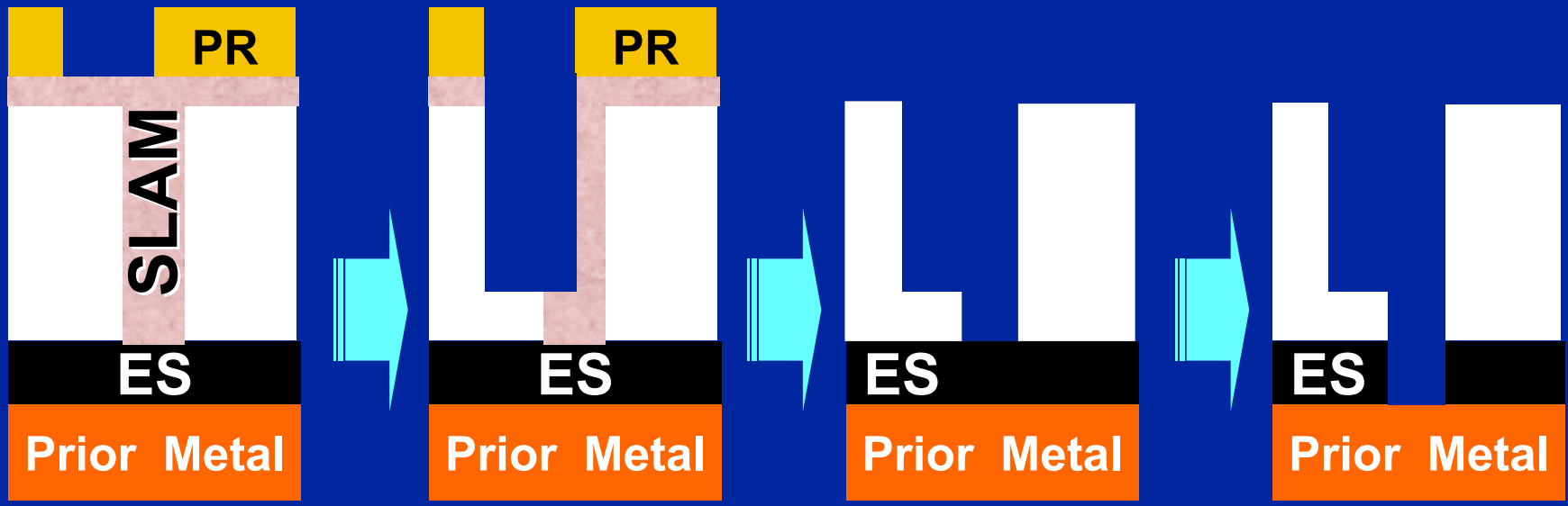
SLAM; Intel's Innovation

- SLAM offers a comprehensive solution to dual-damascene patterning
- Two patents assigned to Intel:
 - Pat. # 6,329,118: SLAM material
 - Pat. # 6,365,529: SLAM-based DD flow
- Honeywell Electronic Materials (HEM) is the supplier for SLAM

SLAM Characteristics

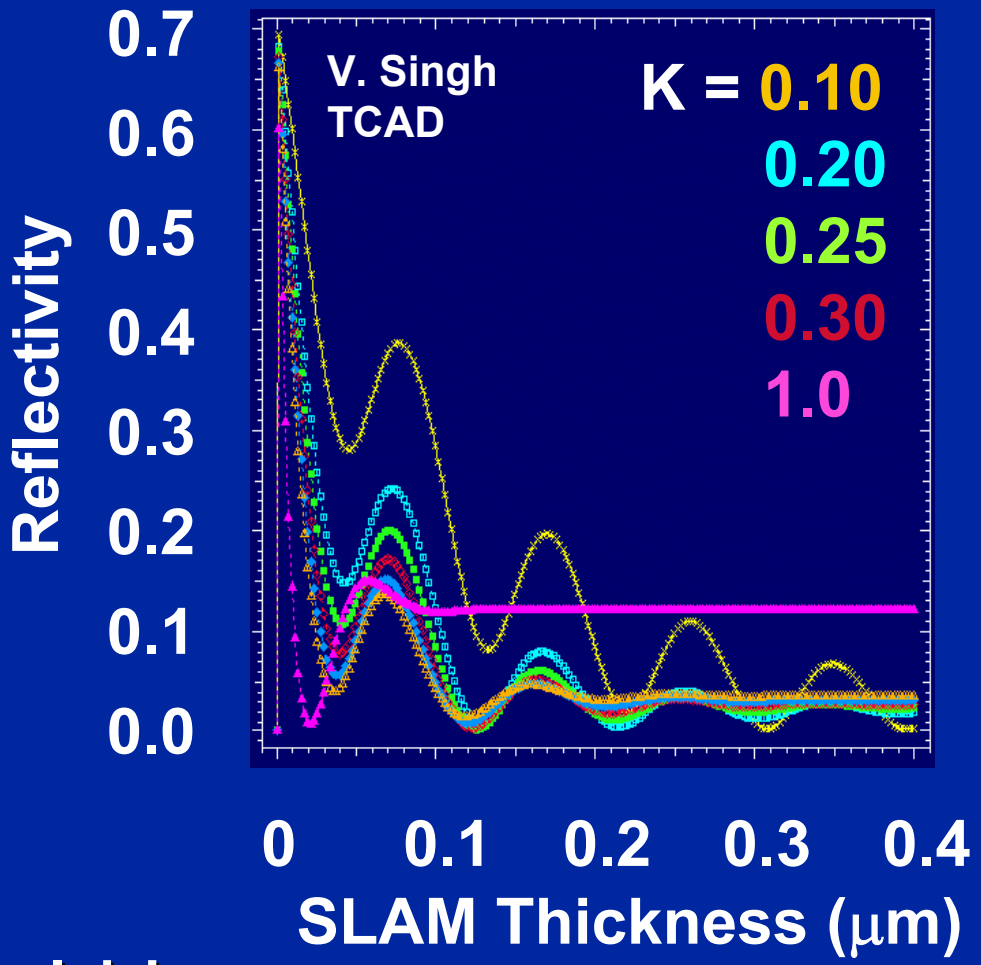
- Capable of completely filling the vias
- High optical absorption at exposure wavelength used in lithography
- Compatible with Litho operations
- Dry etch rate comparable to that of ILD
- To facilitates SLAM removal post trench etch, wet etch rate >> ILD's

SLAM-Assisted Patterning



Trench Litho Trench Etch Trench Cleans ES Etch

Reflectivity Control

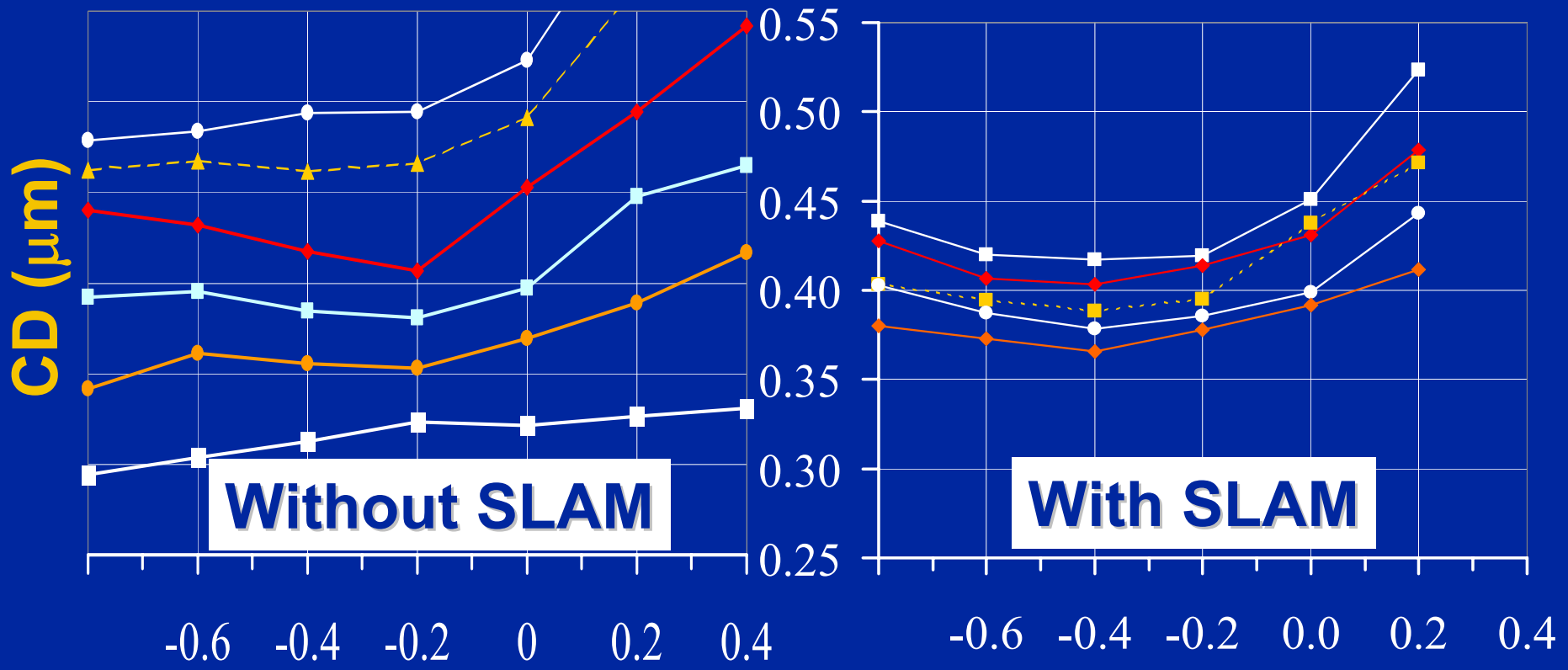


- k (~0.3) keeps reflectivity < 5%
- Dye content in SLAM is adjusted to provide required absorption

SLAM Suppresses Substrate Reflectivity

Lithographic Performance

SLAM improves exposure latitude

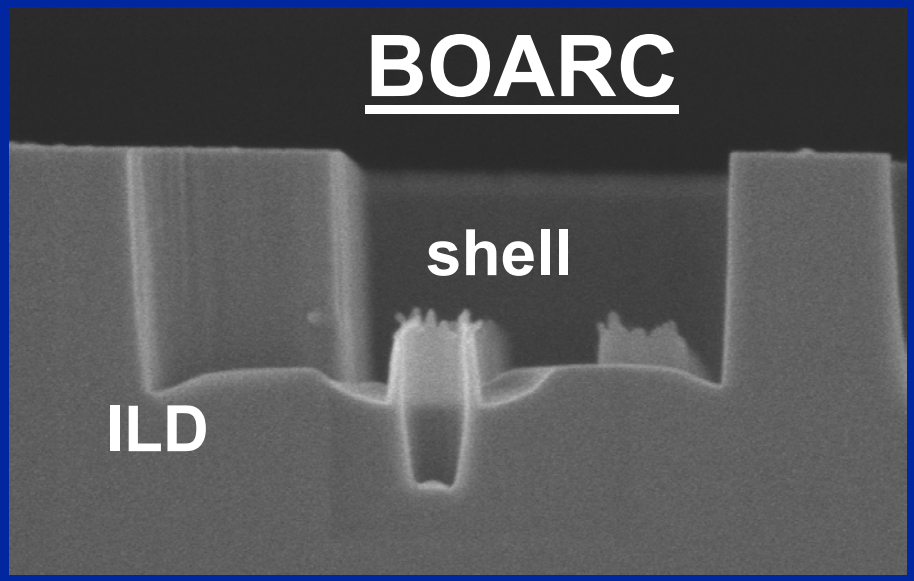


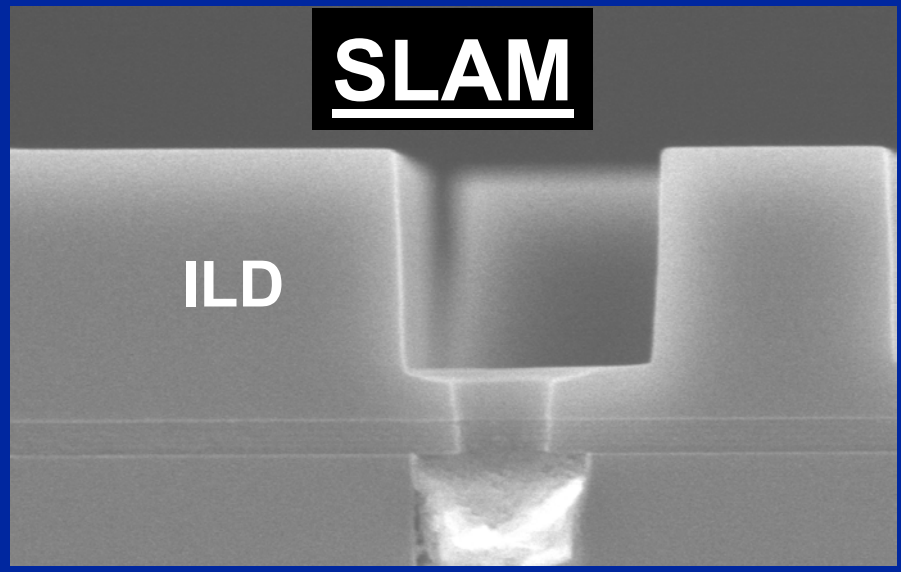
M. Hussein / IITC-2002

SLAM Relaxes Selectivity

- SLAM eliminates the need for ES selectivity during trench etch
 - ES selectivity requirement is confined to via etch
 - Trench etch process may be optimized for profile and etch bias performance

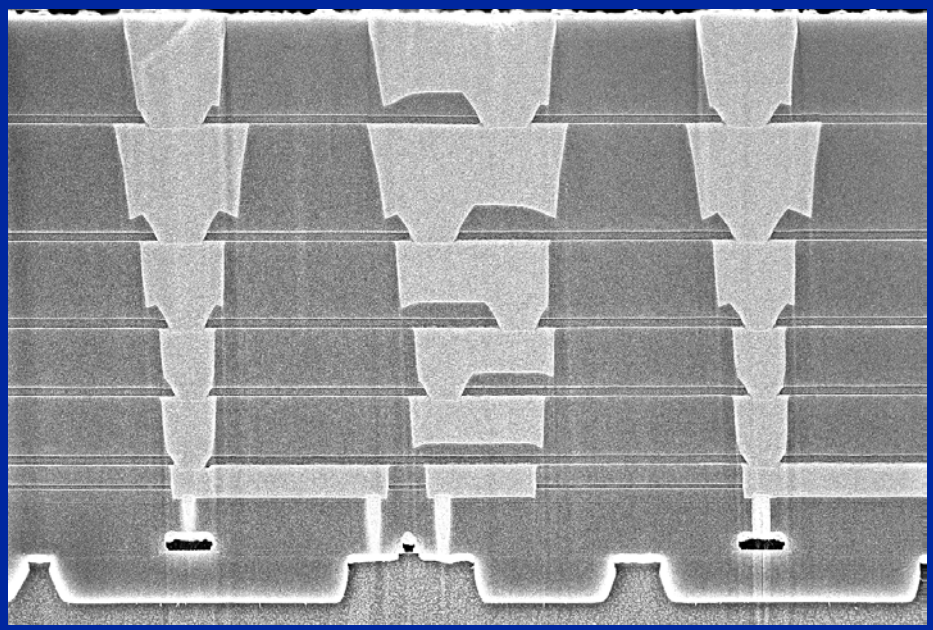
SLAM Eliminates Shells



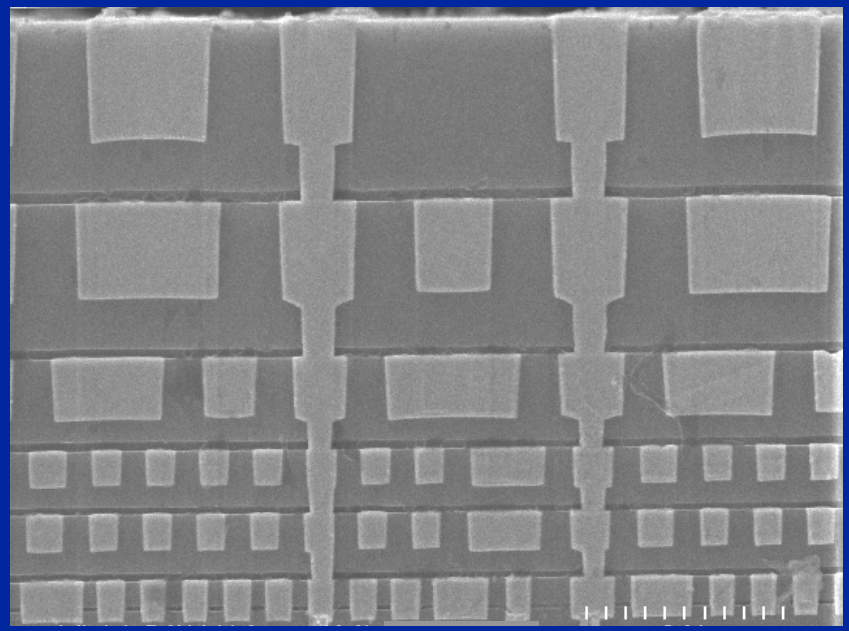


Ability to achieve comparable etch rates between SLAM and ILD eliminates the shell defect problem in a fundamental way

Manufacturability of SLAM



Without SLAM



With SLAM

SLAM-assisted dual damascene patterning is a proven, manufacturable technology

Extendable Technology

- SLAM was initially developed for the 130nm technology node
- We believe that SLAM is extendable to technologies beyond the 130nm node
- SLAM is expected to continue its solid litho and defect performance

Outline

- Key patterning challenges
- BOARC-assisted patterning
- Innovative approach to patterning
- **Conclusion**

Conclusions

- We presented a novel, Intel-invented material and process flow to enable dual damascene patterning
- SLAM eliminates the major failure modes limiting conventional patterning approach
- SLAM-assisted dual damascene patterning is a robust and proven high volume manufacturing technology
- SLAM-assisted dual damascene patterning is extendable beyond the 130nm node

Acknowledgements

- Sam Sivakumar, co-inventor of SLAM
- The 130nm Process Program management and engineers
- Sohail Ahmed, Patterning Manager
- Dr. Joe Kennedy and members of the SLAM development team at Honeywell